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10/699,412	10/31/2003	Josephus C. Ebergen	SUN-P9550	2088

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EXAMINER	
COONEY, ADAM A	

ART UNIT	PAPER NUMBER
2443	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,412	EBERGEN ET AL.	
	Examiner	Art Unit	
	ADAM COONEY	2443	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-18,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the amendment filed on 4/19/2011. Claims 1, 11, and 20 were amended. Claim 21 was added; therefore claims 1-4, 6-9, 11-18, 20 and 21 are pending.

Response to Arguments

Applicant's arguments, see pages 7 and 8, with respect to the rejection of claim 11 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Orsic and Erimli. The examiner would like to note that the applicant has amended the claim to recite "*wherein the acknowledgement signal is generated by logically combining a previous acknowledgement signal generated from the cell and an acknowledgement signal from a neighboring cell with the flow control signal*". The examiner submits that there is no support in the specification for said limitation. The applicant states that support is found throughout the instant application, in particular in Figures 6 and 7 (see applicant's remarks pages 7 and 8). However, there is no such support. In fact, the specification merely states the "controller can define a new clearance-to-send signal for a transmitter as the logical AND of the old clearance-to-send signal for the transmitter and the flow control signal of the receiver". Further, the specification states "each cell is...configured to issue an acknowledgement signal to the corresponding transmitter" (see applicant's specification paragraph 0010) and "the system includes an acknowledgement mechanism configured to confirm the release of the clearance by

resetting the acknowledgement signal" (see applicant's specification paragraph 0014). There is no support showing "*combining a previous acknowledge signal generated from the cell* ***and an acknowledgement signal from a neighboring cell*** (emphasis added)". Erimli teaches a multiport switch may include a receiver, a transmitter, flow control logic, buffer management, token bucket, etc (see Erimli column 4 lines 22-32). A first logic element operates upon mask signals and threshold signals. The first logic element may include multiple logic devices that each generate a flow control signal. A second logic element operates upon flow control signals from the first element (previous signals). The second logic element may generate a flow control signal. The flow control signal from both the first and second logic elements may be sent to the flow control logic (see Erimli column 7 line 39 – column 8 line 15, column 9 lines 5-16 and Figures 3 and 4). Therefore, Orsic in combination with Erimli teaches all the limitations of claim 11, as shown in the rejection below.

Applicant's arguments, see pages 8-10, with respect to the rejection of claim 1 under 35 U.S.C. 103(a) have been fully considered but are not persuasive. Applicant states that neither Orsic, Erimli or the combination of both teaches "*generating the acknowledgement signal by logically combining a previous acknowledge signal from the cell and an acknowledgement signal from a neighboring cell*". As stated above, there is no support for said limitation in the specification. For purposes of examination, the claim is construed as combining the previous acknowledgment signal and an acknowledgement signal from the cell (one cell), as supported by the applicant's specification. Erimli teaches a multiport switch may include a receiver, a transmitter, flow control logic, buffer management, token bucket, etc (see Erimli column 4 lines 22-32). A first logic element operates upon mask signals and threshold signals. The first logic

element may include multiple logic devices that each generate a flow control signal. A second logic element operates upon flow control signals from the first element (previous signals). The second logic element may generate a flow control signal. The flow control signal from both the first and second logic elements may be sent to the flow control logic (see Erimli column 7 line 39 – column 8 line 15, column 9 lines 5-16 and Figures 3 and 4). Therefore, Orsic in combination with Erimli does in fact teach "*generating the acknowledgement signal by logically combining a previous acknowledge signal from the cell and an acknowledgement signal from a neighboring cell*" along with all other limitations, as shown in the rejection below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-4, 6-9, 11-18, 20 and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claims have been amended to recite "*combining a previous acknowledgement signal generated from the cell and an acknowledgement signal from a neighboring cell*". The examiner submits that there is no support in the specification for said limitation. The applicant states that

support is found throughout the instant application, in particular in Figures 6 and 7 (see applicant's remarks pages 7 and 8). However, there is no such support. In fact, the specification merely states the "controller can define a new clearance-to-send signal for a transmitter as the logical AND of the old clearance-to-send signal for the transmitter and the flow control signal of the receiver". Further, the specification states "each cell is...configured to issue an acknowledgement signal to the corresponding transmitter" (see applicant's specification paragraph 0010) and "the system includes an acknowledgement mechanism configured to confirm the release of the clearance by resetting the acknowledgement signal" (see applicant's specification paragraph 0014). There is no support showing "*combining a previous acknowledge signal generated from the cell* ***and an acknowledgement signal from a neighboring cell*** (emphasis added)". For purposes of examination, the claim is construed as combining the previous acknowledgment signal and an acknowledgement signal from the cell (one cell), as supported by the applicant's specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-9, 11-18, 20 and 21 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Orsic in view of Erimli et al. (U.S. 6,842,423 B1).

Regarding claim 1, Orsic teaches a system for regulating communications between a plurality of transmitters (input controllers) and a receiver (output controllers) (see column 3 lines 48-53 and Figure 1; input controller transmits a packet to output controller, therefore input controller is the transmitter and output controller is the receiver), comprising: a plurality of cells (see Figure 1; crosspoint elements, i.e. 107-11 and 107-21), wherein each cell controls communications from a transmitter in the plurality of transmitters to the receiver; wherein the plurality of cells are arranged in a token ring (control ring) that regulates communications from the plurality of transmitters to the receiver; and wherein the presence of a token within a token ring cell indicates that the corresponding transmitter may communicate with the receiver (see column 2 lines 9-35, column 4 lines 16-20 and Figure 1; an array of crosspoint elements each associated with one of the input means and one of the output means, each crosspoint element is associated with its own control ring, the control mechanism is efficient in enabling packet transmission, further each crosspoint element is responsive to a token for switching information from its associated input means to its associated output means). Also, Orsic teaches a signal based on the presence of a token (e-bit) and a signal indicating the receiver is ready to receive from the transmitter (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line) and wherein each cell is configured to receive a request signal from a corresponding transmitter, and in response to the request signal, is configured to issue an acknowledgement signal (grant signal) to the corresponding transmitter which allows the corresponding transmitter to begin transmitting if the cell has the token (see column 3 lines 48-68 through column 4 lines 1-6 and 16-20, also column 5 lines 12-26) and a flow control mechanism in each cell that receives a flow-control signal from the

receiver, wherein the receiver asserts the flow-control signal when the receiver is ready to receive communications (see column 6 lines 28-36; "receiver"/output controller provides flow control and applies a busy signal to stop the flow of packets). Orsic does not teach and wherein the flow control mechanism comprises logic for generating the acknowledgement signal by logically combining a previous acknowledge signal from the cell and an acknowledgement signal from a neighboring cell with the flow-control signal.

However, Erimli does teach such a limitation. According to Erimli, a multiport switch may include a receiver, a transmitter, flow control logic, buffer management, token bucket, etc (see Erimli column 4 lines 22-32). A first logic element operates upon mask signals and threshold signals. The first logic element may include multiple logic devices that each generate a flow control signal. A second logic element operates upon flow control signals from the first element (previous signals). The second logic element may generate a flow control signal. The flow control signal from both the first and second logic elements may be sent to the flow control logic (see Erimli column 7 line 39 – column 8 line 15, column 9 lines 5-16 and Figures 3 and 4).

Therefore, it would have been obvious to a person of ordinary skill in the art to have combined Orsic's teaching of a logic circuit that receives a signal from a flip-flop and a signal from the output controller (receiver) indicating whether its busy or not and then outputs a grant signal to the input controller with Erimli's method of flow control logic, because Orsic teaches that the output controllers provides buffering facilities and flow control (see Orsic column 6 lines 28-36) and Erimli's method of flow control logic is one way to implement flow control.

Regarding claim 2, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches a plurality of receivers (see Figure 1); and a plurality of token rings (see

column 2 lines 32-33 and Figure 1), wherein each token ring passes a corresponding token among token ring cells that control communications from the plurality of transmitters to a receiver corresponding to the token ring (see column 2 lines 13-29, column 3 lines 34-37 and column 4 lines 16-20).

Regarding claim 3, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein the plurality of cells are arranged in a grid (array) wherein a row corresponds to a transmitter and a column corresponds to a receiver (see column 2 lines 25-29 and Figure 1).

Regarding claim 4, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein the communications can include one of: an electrical signal; a mechanical signal; and an optical signal (see column 3 lines 52-58 and Figure 1, it is inherent that when using bus lines, i.e. R and G lines, that an electrical signal is used).

Regarding claim 6, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein each transmitter further comprises a reset mechanism that is configured to release the clearance to communicate with the receiver by resetting the request signal (see column 4 lines 6-8 and column 5 lines 27-30; once transmission of the packet is complete the input controller "resets" by applying a low signal to the R line of the bus).

Regarding claim 7, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein the system further comprises an acknowledgement mechanism configured to confirm the release of the clearance by resetting the acknowledgement signal (see column 4 lines 9-13 and column 5 lines 30-32; the system "confirms the release" by the crosspoint element removing the grant signal from the G line of the bus).

Regarding claim 8, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches an initialization mechanism configured to initialize the single token in the token ring (see column 3 lines 34-35 and column 4 lines 67-68 through column 5 lines 1-4; generates a new "token", E-bit, therefore initializing the E-bit).

Regarding claim 9, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein the system operates asynchronously (see column 5 lines 12-34; input controller requests, waits for and receives grant signal, then transmits packet, therefore asynchronous because it is not simultaneous).

Regarding claim 11, Orsic teaches a method for regulating communications between a plurality of transmitters (input means/input controllers) and a receiver (output means/output controllers) (see column 3 lines 48-53 and Figure 1, i.e. 101-1 and 102-1; input controller transmits a packet to output controller, therefore input controller is the transmitter and output controller is the receiver), comprising: receiving a request signal from a transmitter at a cell (crosspoint element) in a plurality of cells requesting to communicate with the receiver (see column 3 lines 52-62, column 5 lines 16-22 and column 6 lines 3-7); wherein the plurality of cells are arranged in a token ring (control ring) that regulates communications from the plurality of transmitters to the receiver (see column 2 lines 11-24 and Figure 1); and in response to the request signal, issuing an acknowledgement signal (grant signal) to the transmitter which allows the transmitter to begin transmitting if the presence of a token is detected within the cell, wherein the acknowledgement signal is not issued unless the receiver has asserted an enabling signal to the cell that indicates that the receiver is ready to receive data (see column 3 lines 48-68 through column 4 lines 1-6 and 16-20, also column 5 lines 12-26 and 37-53, column 6 lines

15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line; a signal based on the e-bit and a signal indicating the receive is ready to receive from the transmitter) and a flow-control signal has been asserted by the receiver (see column 6 lines 28-36; "receiver"/output controller provides flow control and applies a busy signal to stop the flow of packets). Orsic does not teach wherein the acknowledgement signal is generated by logically combining a previous acknowledgement signal generated from the cell and an acknowledgement signal from a neighboring cell with the flow control signal.

However, Erimli does teach such a limitation. According to Erimli, a multiport switch may include a receiver, a transmitter, flow control logic, buffer management, token bucket, etc (see Erimli column 4 lines 22-32). A first logic element operates upon mask signals and threshold signals. The first logic element may include multiple logic devices that each generate a flow control signal. A second logic element operates upon flow control signals from the first element (previous signals). The second logic element may generate a flow control signal. The flow control signal from both the first and second logic elements may be sent to the flow control logic (see Erimli column 7 line 39 – column 8 line 15, column 9 lines 5-16 and Figures 3 and 4).

Therefore, it would have been obvious to a person of ordinary skill in the art to have combined Orsic's teaching of a logic circuit that receives a signal from a flip-flop and a signal from the output controller (receiver) indicating whether its busy or not and then outputs a grant signal to the input controller with Erimli's method of flow control logic, because Orsic teaches that the output controllers provides buffering facilities and flow control (see Orsic column 6 lines 28-36) and Erimli's method of flow control logic is one way to implement flow control.

Regarding claim 12, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein the plurality of cells include a plurality of token rings (see column 2 lines 32-33 and Figure 1), wherein each token ring passes a corresponding token among token ring cells that control communications from the plurality of transmitters to a receiver corresponding to the token ring (see Orsic column 2 lines 13-29, column 3 lines 34-37 and column 4 lines 16-20).

Regarding claim 13, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein a plurality of cells that regulate communications between the transmitters and receivers are arranged in a grid (array) wherein a row corresponds to a transmitter and a column corresponds to a receiver (see Orsic column 2 lines 25-29 and Figure 1).

Regarding claim 14, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein the communications can include one of: an electrical signal; a mechanical signal; and an optical signal (see Orsic column 3 lines 52-58 and Figure 1, it is inherent that using bus lines, i.e. R and G lines, that an electrical signal is used).

Regarding claim 15, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches revoking the permission for the transmitter to communicate with the receiver when the transmitter resets the request signal (see Orsic column 4 lines 6-8 and column 5 lines 27-32).

Regarding claim 16, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches resetting the acknowledgement signal to confirm the revocation of the

permission for the transmitter to communicate with the receiver (see Orsic column 4 lines 9-13 and column 5 lines 30-32).

Regarding claim 17, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches initializing the token in the token ring (see Orsic column 3 lines 34-35 and column 4 lines 67-68 through column 5 lines 1-4).

Regarding claim 18, Orsic and Erimli disclose the invention substantially as claimed. Further, Orsic teaches wherein the system operates asynchronously (see Orsic column 5 lines 12-34; input controller requests, waits for and receives grant signal, then transmits packet, therefore asynchronous because it is not simultaneous).

Regarding claim 20, Orsic teaches a multi-processor system, comprising: a plurality of processors (see column 3 lines 1-9 and Figure 1, i.e. 11 and 21; input devices and output devices include terminal equipment, therefore the terminals are the processors); a plurality of transmitters (input controllers) associated with the processors; a plurality of receivers (output controllers) associated with the plurality of processors (see column 3 lines 48-53 and Figure 1; input controller transmits a packet to output controller, therefore input controller is the transmitter and output controller is the receiver); a plurality of cells (see Figure 1; crosspoint elements, i.e. 107-11 and 107-21), wherein each cell controls communications from a transmitter in the plurality of transmitters to a receiver; wherein the plurality of cells are arranged in a token ring (control ring) that regulates communications from the plurality of transmitters to the receiver; and wherein the presence of a token within a token ring cell indicates that the corresponding transmitter may communicate with the receiver (see column 2 lines 9-35, column 4 lines 16-20 and Figure 1; an array of crosspoint elements each associated with one of the input means and one of the output

means, each crosspoint element is associated with its own control ring, the control mechanism is efficient in enabling packet transmission, further each crosspoint element is responsive to a token for switching information from its associated input means to its associated output means). Also, Orsic teaches a signal based on the presence of a token (e-bit) and a signal indicating the receiver is ready to receive from the transmitter (see Orsic column 5 lines 37-53, column 6 lines 15-18 and Figure 2; item 108 Flip Flop, item 111 Logic Circuit and item 104-1 B-line) and wherein each cell is configured to receive a request signal from a corresponding transmitter, and in response to the request signal, is configured to issue an acknowledgement signal (grant signal) to the corresponding transmitter which allows the corresponding transmitter to begin transmitting if the cell has the token (see column 3 lines 48-68 through column 4 lines 1-6 and 16-20, also column 5 lines 12-26) and a flow control mechanism in each cell that receives a flow-control signal from the receiver, wherein the receiver asserts the flow-control signal when the receiver is ready to receive communications (see column 6 lines 28-36; "receiver"/output controller provides flow control and applies a busy signal to stop the flow of packets). Orsic does not teach and wherein the flow control mechanism comprises logic for generating the acknowledgement signal by logically combining a previous acknowledge signal from the cell and an acknowledgement signal from a neighboring cell with the flow-control signal.

However, Erimli does teach such a limitation. According to Erimli, a multiport switch may include a receiver, a transmitter, flow control logic, buffer management, token bucket, etc (see Erimli column 4 lines 22-32). A first logic element operates upon mask signals and threshold signals. The first logic element may include multiple logic devices that each generate a flow control signal. A second logic element operates upon flow control signals from the first

element (previous signals). The second logic element may generate a flow control signal. The flow control signal from both the first and second logic elements may be sent to the flow control logic (see Erimli column 7 line 39 – column 8 line 15, column 9 lines 5-16 and Figures 3 and 4).

Therefore, it would have been obvious to a person of ordinary skill in the art to have combined Orsic's teaching of a logic circuit that receives a signal from a flip-flop and a signal from the output controller (receiver) indicating whether its busy or not and then outputs a grant signal to the input controller with Erimli's method of flow control logic, because Orsic teaches that the output controllers provides buffering facilities and flow control (see Orsic column 6 lines 28-36) and Erimli's method of flow control logic is one way to implement flow control.

Regarding claim 21, Orsic and Erimli disclose the invention substantially as claimed. Further, Erimli teaches wherein the acknowledgement signal from the neighboring cell is generated by combining a previous acknowledge signal from the neighboring cell and an acknowledgement signal from a cell neighboring the neighboring cell with a flow-control signal received by the neighboring cell from a receiver for the neighboring cell (see Erimli column 7 line 39 – column 8 line 15, column 9 lines 5-16 and Figures 3 and 4). The same motivation used in combining Orsic and Erimli in claim 3, applies equally as well to claim 21.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADAM COONEY whose telephone number is (571)270-5653. The examiner can normally be reached on Monday-Thursday and every other Friday from 730AM-5PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tonia Dollinger can be reached on 571-272-4170. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. C./
Examiner, Art Unit 2443
6/21/2011

/TONIA L.M. DOLLINGER/
Supervisory Patent Examiner, Art Unit 2443